WHAT IS CLAIMED IS:

1. An electronic circuit, comprising a plurality of first D/A converters, wherein each first D/A converter is provided with:

an offset memory means for memorizing offset correction digital data, and

an operation means for adding or subtracting the offset correction digital data to a digital input signal to the D/a converter.

2. An electronic circuit according to Claim 1, further including at least one A/D converter unit for generating the offset correction digital data to be memorized in the offset memory means.

3. An electronic circuit, comprising a plurality of first D/A converters and at least one correction A/D converter unit, wherein

each first D/A converter is provided with an offset memory means for memorizing offset correction digital data, and an operation means for adding or subtracting the offset correction digital data to a digital input signal to the D/A converter, and

said correction A/D converter unit includes a comparative data generating circuit having a plurality of bits and sequentially outputting plural-bit data while changing the plural-bit data sequentially from

its upper bits, an adder means for adding a digital input signal and an output from the comparative data-generating circuit, a second D/A converter for converting a digital output from the adder means into an analog signal, a comparator means for comparing the analog signal with an analog output from each first D/A converter, and an encoder means for generating offset correction digital data to be memorized in the offset memory means based on an output of the comparator means.

4. An electronic circuit according to Claim 1 or 3, wherein each D/A converter has a capacity for receiving totally m bits larger than n bits of the digital input signal by at least one bit ($m-n \geq 1$), so as to input lower L bits ($L \geq 1$) of the offset correction digital data of k bits to lower L bits of the D/A converter and input a digital signal obtained by adding the n-bit digital input signal and upper ($k-L$) bits of the offset correction digital data to upper ($m-L$) bits of the D/A converter.

5. An electronic circuit according to Claim 1 or 3, wherein each first D/A converter is provided with a reference voltage generating circuit capable of generating a plurality of successive levels of reference voltages, so that i-th and (i+2)-th levels

of reference voltages among the successive levels of reference voltages are selected based on upper j bits of the n-bit digital input signal, and a voltage between the i-th and (i+2)-th reference voltages is further divided based on lower (n-j) bits of the n-bit digital input signal.

6. A liquid crystal display apparatus, comprising: an active matrix substrate having thereon a plurality of scanning lines, a plurality of signal lines and pixel electrodes each connected via a switch to an intersection of the scanning lines and the signal lines, a counter substrate disposed with a spacing from the active matrix, a liquid crystal sandwiched between the active matrix substrate and the counter substrate, and an electronic circuit according to Claim 1 or 3 disposed so as to supply picture signals to the signal lines.

7. A liquid crystal display apparatus according to Claim 6, wherein the electronic circuit is disposed on a common substrate with the active matrix substrate.

8. A liquid crystal apparatus, comprising:

a liquid crystal device comprising an active matrix substrate having thereon a plurality of signal

lines arranged in columns, a plurality of scanning lines arranged rows, and pixel electrodes each connected via a pixel switch to an intersection of the signal lines and the scanning lines so as to supply picture signals to the pixel electrodes via the signal lines, a counter substrate disposed opposite to the active matrix substrate, and a liquid crystal disposed between the active matrix substrate and the counter substrate, and

drive means for driving the liquid crystal devices, wherein said drive means including:

a first common signal line and a second common signal line for supplying the picture signals,

picture signal-supplying means for supplying picture signals of one polarity to the first common signal line and picture signals of the other polarity to the second common signal line,

a first and a second transfer switch provided to each column signal line for selectively supplying one of picture signals supplied to the first and second common signal lines to each column signal line, and

column inversion drive means for:

in a first frame, selectively turning on the first transfer switches for odd-numbered column signal lines and the second transfer switches for even-numbered column signal lines, and in a second frame,

selectively turning on the second transfer switches for odd-numbered column signal lines and the first transfer switches for even-numbered column signal lines.

9. A liquid crystal apparatus, comprising:

a liquid crystal device comprising an active matrix substrate having thereon a plurality of signal lines arranged in columns, a plurality of scanning lines arranged rows, and pixel electrodes each connected via a pixel switch to an intersection of the signal lines and the scanning lines so as to supply picture signals to the pixel electrodes via the signal lines, a counter substrate disposed opposite to the active matrix substrate, and a liquid crystal disposed between the active matrix substrate and the counter substrate, and

drive means for driving the liquid crystal devices, wherein said drive means including:

a first common signal line and a second common signal line for supplying the picture signals,

picture signal-supplying means for supplying picture signals of one polarity to the first common signal line and picture signals of the other polarity to the second common signal line,

a first and a second transfer switch provided to each column signal line for selectively supplying

one of picture signals supplied to the first and second common signal lines to each column signal line, and

dot inversion drive means for:

in a first frame, selectively turning on the first transfer switches for odd-numbered column signal lines and the second transfer switches for even-numbered column signal lines at the time of scanning odd-numbered scanning lines, and selectively turning on the second transfer switches for odd-numbered column signal lines and the first transfer switches for even-numbered column signal lines at the time of scanning even-numbered scanning lines; and

in a second frame, selectively turning on the second transfer switches for odd-numbered column signal lines and the first transfer switches for even-numbered column signal lines at the time of scanning odd-numbered scanning lines, and selectively turning on the first transfer switches for odd-numbered column signal lines and the second transfer switches for even-numbered column signal lines at the time of scanning even-numbered scanning lines.

10. A liquid crystal apparatus according to Claim 8 or 9, wherein the first transfer switches comprise a transistor of a first conductivity type and the second transfer switches comprise a transistor of a

second conductivity type different from the first conductivity type.

11. A liquid crystal apparatus according to Claim 8 or 9, wherein the picture signal supply means includes first and second picture signal-generating means for generating positive-polarity picture signals and negative-polarity picture signals, respectively, supplied to the first and second common signal lines, respectively; the first picture signal generating means generate picture signals in a range between a highest voltage and a central voltage supplied to the pixel electrodes; the second picture signal-generating means generates picture signals in a range between the central voltage and a lowest voltage supplied to the pixel electrodes; the first and second picture signal-garnering means are operated at different supply voltages; the supply voltages for the first picture signal-generating means are set to be the highest voltage + α and the central voltage - α; and the supply voltages for the second picture signal-generating means are set to be the central voltage + α and the lowest voltage - α, wherein α denotes a voltage lowering margin due to an internal resistance in the picture signal-generating means.

12. A liquid crystal apparatus according to Claim

11, wherein α is in the range of 0 volt to 1 volt.

13. A liquid crystal apparatus according to Claim 8, wherein the first and second transfer switches and the picture signal supply means are disposed on a common substrate with the active matrix substrate.

14. A liquid crystal apparatus according to Claim 13, wherein the active matrix substrate comprises an insulating substrate.

15. A liquid crystal apparatus according to Claim 13, wherein the active matrix substrate comprises a single crystal substrate.